

Equipment problems

Notes on back

revolution

May 04 Sat

Revolution Hall

set page 1 of 5

Kit No:	Director:	Cam Op:	Audio op:	File count: _____
Pre-Day check: <input type="checkbox"/> Replace Batteries in mics Sound levels: <input type="checkbox"/> L-PA <input type="checkbox"/> R-cam mic <input type="checkbox"/> System date and time.		Post production: <input type="checkbox"/> Files synked Edit by: <input type="checkbox"/> Set Scanned Review by: <input type="checkbox"/> Edit - set done <input type="checkbox"/> Review - done		

Sound check Title: Welcome
 Presenter(s):

Start: HH_MM_SS

09:00 (9:00 am)

Length: 0:10:0

End: HH_MM_SS Released: yes no.

misc.

09:10 (9:10 am) Presenter email:

id: 14798 conf: 0

Presenter initials for intent to release: _____

Edit Review

Sound check Title: FOSSi Foundation Update
 Presenter(s):

Start: HH_MM_SS

09:10 (9:10 am)

Length: 0:20:0

End: HH_MM_SS Released: yes no.

misc.

09:30 (9:30 am) Presenter email:

id: 14799 conf: 1

Presenter initials for intent to release: _____

Edit Review

Sound check Title: Diagrams and system visualisation in chip design
 Presenter(s): Aliaksei Chapyzenka

Start: HH_MM_SS

09:30 (9:30 am)

Length: 0:30:0

End: HH_MM_SS Released: yes no.

misc.

10:00 (10:00 am) Presenter email:

id: 14800 conf: 2

Presenter initials for intent to release: _____

Edit Review

Sound check

Unscheduled

Start: _____

Lighting Talks

Keynote

misc.

Added to Veyepar

End: _____

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Sound check

Title: Netlistsvg: How to Draw a Better Schematic than Graphviz

Presenter(s): Neil Turley

Start: HH_MM_SS

10:00 (10:00 am)

Length: 0:30:0

End: HH_MM_SS

10:30 (10:30 am)

id:14801 conf: 3

Presenter email:

misc.

Edit

Review

Sound check

Title: Lessons learned customising the Rocket RISC-V core

Presenter(s): Julius Baxter

Start: HH_MM_SS

10:50 (10:50 am)

Length: 0:20:0

End: HH_MM_SS

11:10 (11:10 am)

id:14802 conf: 4

Presenter email:

misc.

Edit

Review

Sound check

Title: Higher-Order Hardware Design with Chisel 3

Presenter(s): Jack Koenig

Start: HH_MM_SS

11:10 (11:10 am)

Length: 0:30:0

End: HH_MM_SS

11:40 (11:40 am)

id:14803 conf: 5

Presenter email:

misc.

Edit

Review

Sound check

Title: The fusion of high-level synthesis with event-oriented hardware description (myhdl)

Presenter(s): Christopher Felton

Start: HH_MM_SS

11:40 (11:40 am)

Length: 0:30:0

End: HH_MM_SS

12:10 (12:10 pm)

id:14804 conf: 6

Presenter email:

misc.

Edit

Review

Sound check

Unscheduled

Start: _____

Lighting Talks

Keynote

misc.

Added to Veyepar

End: _____

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Sound check

Title: JuxtaPiton: The First Open-Source, Heterogeneous-ISA Processor

Presenter(s): Katie Lim

Start: HH_MM_SS

13:30 (1:30 pm)

Length: 0:20:0

End: HH_MM_SS

13:50 (1:50 pm)

id: 14805 conf: 7

Presenter email:

misc.

Edit

Review

Sound check

Title: OpenPiton+Ariane: Making Ariane Multicore with OpenPiton's P-Mesh

Presenter(s): Jonathan Balkind

Start: HH_MM_SS

13:50 (1:50 pm)

Length: 0:20:0

End: HH_MM_SS

Released: yes no.

Presenter email:

misc.

14:10 (2:10 pm)

id: 14806 conf: 8

Presenter initials for intent to release: _____

Edit

Review

Sound check

Title: Lessons Learned from Open-Sourcing NVDLA

Presenter(s): Joshua Wise

Start: HH_MM_SS

14:10 (2:10 pm)

Length: 0:20:0

End: HH_MM_SS

Released: yes no.

Presenter email:

misc.

14:30 (2:30 pm)

id: 14807 conf: 9

Presenter initials for intent to release: _____

Edit

Review

Sound check

Title: DVKit: An Integrated Development Environment for Design and Verification Engineers

Presenter(s): Matthew Ballance

Start: HH_MM_SS

14:30 (2:30 pm)

Length: 0:20:0

End: HH_MM_SS

Presenter email:

misc.

14:50 (2:50 pm)

id: 14808 conf: 10

Edit

Review

Sound check

Unscheduled

Start: _____

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misc.

Added to Veyepar

End: _____

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Sound check

Title: Live Graph infrastructure for Synthesis and Simulation

Presenter(s): Jose Renau

Start: HH_MM_SS

15:30 (3:30 pm)

Length: 0:30:0

End: HH_MM_SS

16:00 (4:00 pm)
id: 14809 conf: 11

Presenter email:

misc.

Edit Review

Sound check

Title: The Berkeley-Out-of-Order-Machine: An Open Source Synthesizable High-Performance RISC-V Processor

Presenter(s): Jerry Zhao, Abe Gonzalez, Ben Korpan

Start: HH_MM_SS

16:00 (4:00 pm)

Length: 0:30:0

End: HH_MM_SS

16:30 (4:30 pm)
id: 14810 conf: 12

Presenter email:

misc.

Edit Review

Sound check

Title: FireSim: Open-Source Easy-to-use FPGA-Accelerated Cycle-Exact Hardware Simulation in the Cloud

Presenter(s): David Biancolin, Alon Amid

Start: HH_MM_SS

16:30 (4:30 pm)

Length: 0:30:0

End: HH_MM_SS

17:00 (5:00 pm)
id: 14811 conf: 13

Presenter email:

misc.

Edit Review

Sound check

Title: How I started learning FPGA: My journey writing a GameBoy in Verilog

Presenter(s): Wenting Zhang

Start: HH_MM_SS

17:30 (5:30 pm)

Length: 0:30:0

End: HH_MM_SS

18:00 (6:00 pm)
id: 14812 conf: 14

Presenter email:

misc.

Edit Review

Sound check

Unscheduled

Start: _____

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Added to Veyepar

End: _____

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Sound check

Title: Emulation of vintage integrated circuits through die analysis and reverse-EDA

Presenter(s): Cole Johnson

Start: HH_MM_SS

18:00 (6:00 pm)

Length: 0:30:0

End: HH_MM_SS

18:30 (6:30 pm)

id: 14813 conf: 15

Presenter email:

misc.

Edit Review

Sound check

Title: Mingle, drinks

Presenter(s):

Start: HH_MM_SS

18:20 (6:20 pm)

Length: 0:30:0

End: HH_MM_SS

18:50 (6:50 pm)

id: 14814 conf: 16

Released: yes no.

Presenter email:

Presenter initials for intent to release: _____

misc.

Edit Review

NOT Released

Sound check

Unscheduled

Start: _____

Lighting Talks

Keynote

misc.

Added to Veyepar

End: _____

Released: yes no.

Presenter initials for intent to release: _____

Edit Review