start:09:00 end:09:10 Len: 0:10:0 id: 147

Welcome

Welcome

Veyepar: TalkSigns.rfxml

start:09:10 end:09:30 Len: 0:20:0 id: 147

FOSSi Foundation Update

FOSSi Foundation Update

Veyepar: TalkSigns.rfxml

start:09:30 end:10:00 Len: 0:30:0 id: 148

Diagrams and system visualisation in chip design

Aliaksei Chapyzhenka

Diagrams and system visualisation in chip design

Aliaksei Chapyzhenka

Veyepar: TalkSigns.rfxml

start: 10:00 end: 10:30 Len: 0:30:0 id: 148

Netlistsvg: How to Draw a Better Schematic than Graphviz

Neil Turley

Netlistsvg: How to Draw a Better Schematic than Graphviz

Neil Turley

Veyepar: TalkSigns.rfxml

start: 10:50 end: 11:10 Len: 0:20:0 id: 148

Lessons learned customising the Rocket RISC-V core

Julius Baxter

Lessons learned customising the Rocket RISC-V core

Julius Baxter

Veyepar: TalkSigns.rfxml

start: 11:10 end: 11:40 Len: 0:30:0 id: 148

Higher-Order Hardware Design with Chisel 3

Jack Koenig

Higher-Order Hardware Design with Chisel 3

Jack Koenig

Veyepar: TalkSigns.rfxml

start: 11:40 end: 12:10 Len: 0:30:0 id: 148

The fusion of high-level synthesis with event-oriented hardware description (myhdl)

Christopher Felton

The fusion of high-level synthesis with event-oriented hardware description (my

Christopher Felton

Veyepar: TalkSigns.rfxml

start: 13:30 end: 13:50 Len: 0:20:0 id: 148

JuxtaPiton: The First Open-Source, Heterogeneous-ISA Processor

Katie Lim

JuxtaPiton: The First Open-Source, Heterogeneous-ISA Processor

Katie Lim

Veyepar: TalkSigns.rfxml

start: 13:50 end: 14:10 Len: 0:20:0 id: 148

OpenPiton+Ariane: Making Ariane Multicore with OpenPiton’s P-Mesh

Jonathan Balkind

OpenPiton+Ariane: Making Ariane Multicore with OpenPiton’s P-Mesh

Jonathan Balkind

Veyepar: TalkSigns.rfxml

start: 14:10 end: 14:30 Len: 0:20:0 id: 148

Lessons Learned from Open-Sourcing NVDLA

Joshua Wise

Lessons Learned from Open-Sourcing NVDLA

Joshua Wise

Veyepar: TalkSigns.rfxml

start: 14:30 end: 14:50 Len: 0:20:0 id: 148

DVKit: An Integrated Development Environment for Design and Verification Engineers

Matthew Ballance

DVKit: An Integrated Development Environment for Design and Verification En

Matthew Ballance

Veyepar: TalkSigns.rfxml

start: 15:30 end: 16:00 Len: 0:30:0 id: 148

Live Graph infrastructure for Synthesis and Simulation

Jose Renau

Live Graph infrastructure for Synthesis and Simulation

Jose Renau

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:30 Len: 0:30:0 id: 148

The Berkeley-Out-of-Order-Machine: An Open Source Synthesizable High-Performance RISC-V Processor

Jerry Zhao, Abe Gonzalez, Ben Korpan

The Berkeley-Out-of-Order-Machine: An Open Source Synthesizable High-Per

Jerry Zhao, Abe Gonzalez, Ben Korpan

Veyepar: TalkSigns.rfxml

start: 16:30 end: 17:00 Len: 0:30:0 id: 148

FireSim: Open-Source Easy-to-use FPGA-Accelerated Cycle-Exact Hardware Simulation in the Cloud

David Biancolin, Alon Amid

FireSim: Open-Source Easy-to-use FPGA-Accelerated Cycle-Exact Hardware

David Biancolin, Alon Amid

Veyepar: TalkSigns.rfxml

start: 17:30 end: 18:00 Len: 0:30:0 id: 148

How I started learning FPGA: My journey writing a GameBoy in Verilog

Wenting Zhang

How I started learning FPGA: My journey writing a GameBoy in Verilog

Wenting Zhang

Veyepar: TalkSigns.rfxml

start: 18:00 end: 18:30 Len: 0:30:0 id: 148

Emulation of vintage integrated circuits through die analysis and reverse-EDA

Cole Johnson

Emulation of vintage integrated circuits through die analysis and reverse-EDA

Cole Johnson

Veyepar: TalkSigns.rfxml

start: 18:20 end: 18:50 Len: 0:30:0 id: 148

Mingle, drinks

Mingle, drinks

Veyepar: TalkSigns.rfxml

start: 09:30 end: 10:00 Len: 0:30:0 id: 148

BaseJump STL: a Standard Template Library for Hardware Design

Daniel Petrisko

BaseJump STL: a Standard Template Library for Hardware Design

Daniel Petrisko

Veyepar: TalkSigns.rfxml

start: 10:00 end: 10:30 Len: 0:30:0 id: 148

OSVVM, VHDL's #1 FPGA Verification Library

Jim Lewis

OSVVM, VHDL's #1 FPGA Verification Library

Jim Lewis

Veyepar: TalkSigns.rfxml

start: 10:30 end: 11:00 Len: 0:30:0 id: 148

Verifying Open-Source Silicon with SystemVerilog: Getting in on the Ground Floor

Matthew Ballance

Verifying Open-Source Silicon with SystemVerilog: Getting in on the Ground Fl

Matthew Ballance

Veyepar: TalkSigns.rfxml

start: 11:20 end: 11:40 Len: 0:20:0 id: 148

RISC-V in Debian

Vagrant Cascadian

RISC-V in Debian

Vagrant Cascadian

Veyepar: TalkSigns.rfxml

start: 11:40 end: 12:10 Len: 0:30:0 id: 148

Lightning Talks

Lightning Talks

Veyepar: TalkSigns.rfxml

start: 11:49 end: 12:01 Len: 00:12:00 id: 148

Hermes-Lite: Amateur Radio SDR

Steve Haynal

Hermes-Lite: Amateur Radio SDR

Steve Haynal

Veyepar: TalkSigns.rfxml

start: 12:01 end: 12:29 Len: 00:28:00 id: 148

Tim has too many projects - LatchUp Edition

Tim 'mithro' Ansell

Tim has too many projects - LatchUp Edition

Tim 'mithro' Ansell

Veyepar: TalkSigns.rfxml

start: 13:20 end: 13:50 Len: 0:30:0 id: 148

FuseSoC - Cores have never been so much fun

Olof Kindgren

FuseSoC - Cores have never been so much fun

Olof Kindgren

Veyepar: TalkSigns.rfxml

start: 13:50 end: 14:20 Len: 0:30:0 id: 148

DUH: document and tools for HW design reuse

Aliaksei Chapyzhenka

DUH: document and tools for HW design reuse

Aliaksei Chapyzhenka

Veyepar: TalkSigns.rfxml

start: 14:20 end: 14:50 Len: 0:30:0 id: 148

Nyuzi: An Open Source GPGPU Processor

Jeff Bush

Nyuzi: An Open Source GPGPU Processor

Jeff Bush

Veyepar: TalkSigns.rfxml

start: 15:10 end: 15:40 Len: 0:30:0 id: 148

OpenRAM: An Open Source Memory Compiler

Matthew Guthaus

OpenRAM: An Open Source Memory Compiler

Matthew Guthaus

Veyepar: TalkSigns.rfxml

start: 15:40 end: 16:10 Len: 0:30:0 id: 148

SYZYGY: An Open Standard For Semiconductor Evaluation

Tom McLeod

SYZYGY: An Open Standard For Semiconductor Evaluation

Tom McLeod

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:20 Len: 0:20:0 id: 148

Open-Source FPGA tools, how and why?

Piotr Esden-Tempski

Open-Source FPGA tools, how and why?

Piotr Esden-Tempski

Veyepar: TalkSigns.rfxml