start: 13:30 end: 13:50 Len: 00:20:00 id: 152

FireSim: A Scalable Platform for FPGA-Accelerated Simulation, Debugging, Profiling of RTL Designs

Sagar Karandikar

FireSim: A Scalable Platform for FPGA-Accelerated Simulation, Debugging, Pr

Sagar Karandikar

Veyepar: TalkSigns.rfxml

start: 14:00 end: 14:20 Len: 00:20:00 id: 152

bsg_tag: A minimal open-source ASIC configuration bus

Dan Petrisko

bsg_tag: A minimal open-source ASIC configuration bus

Dan Petrisko

Veyepar: TalkSigns.rfxml

start: 15:00 end: 15:20 Len: 00:20:00 id: 152

OmniXtend: coherent scaleout over commodity fabrics

Dejan Vucinic

OmniXtend: coherent scaleout over commodity fabrics

Dejan Vucinic

Veyepar: TalkSigns.rfxml

start: 15:30 end: 15:50 Len: 00:20:00 id: 152

Hammer: A Modular and Reusable Physical Design Flow Tool

Nayiri Krzysztofowicz

Hammer: A Modular and Reusable Physical Design Flow Tool

Nayiri Krzysztofowicz

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:20 Len: 00:20:00 id: 152

CIRCT: Open Source Circuit IR Compilers and Tools

Mike Urbach

CIRCT: Open Source Circuit IR Compilers and Tools

Mike Urbach

Veyepar: TalkSigns.rfxml

start: 17:00 end: 17:20 Len: 00:20:00 id: 152

Accelerating Chisel Development

Jack Koenig

Accelerating Chisel Development

Jack Koenig

Veyepar: TalkSigns.rfxml

start: 17:30 end: 17:50 Len: 00:20:00 id: 152

set page 7 of 36

Open-Source HW Commercial Adoption

Rick O'Connor

Open-Source HW Commercial Adoption

Rick O'Connor

Veyepar: TalkSigns.rfxml

start:08:30 end:08:50 Len: 00:20:00 id: 152

A UCSC Professor's path through Open-Source Hardware

Jose Renau

A UCSC Professor's path through Open-Source Hardware

Jose Renau

Veyepar: TalkSigns.rfxml

start:08:55 end:09:15 Len: 00:20:00 id: 152

So You Want to be an Open Sourcerer?

Dustin Richmond

So You Want to be an Open Sourcerer?

Dustin Richmond

Veyepar: TalkSigns.rfxml

start:08:55 end:09:15 Len: 00:20:00 id: 152

If You Build It, Who Will Come?

Scott Beamer

If You Build It, Who Will Come?

Scott Beamer

Veyepar: TalkSigns.rfxml

start:09:20 end:09:40 Len: 00:20:00 id: 152

Yet Another UCSC Professor’s path through Open-Source Hardware

Matt Guthaus

Yet Another UCSC Professor’s path through Open-Source Hardware

Matt Guthaus

Veyepar: TalkSigns.rfxml

start:09:45 end:10:05 Len: 00:20:00 id: 152

Tapeout-in-a-Semester: The Organization of Berkeley's Tapeout Course

Jerry Zhao

Tapeout-in-a-Semester: The Organization of Berkeley's Tapeout Course

Jerry Zhao

Veyepar: TalkSigns.rfxml

start: 10:10 end: 10:30 Len: 00:20:00 id: 152

Fearless Hardware Design

Rachit Nigam

Fearless Hardware Design

Rachit Nigam

Veyepar: TalkSigns.rfxml

start: 11:00 end: 11:20 Len: 00:20:00 id: 152

Minimax - a Compressed-First, Microcoded RISC-V CPU

Graeme Smecher

Minimax - a Compressed-First, Microcoded RISC-V CPU

Graeme Smeche

Veyepar: TalkSigns.rfxml

start: 11:30 end: 11:50 Len: 00:20:00 id: 152

Open Source Brain-Inspired Neuromorphic Software and Hardware

Jason Eshraghian

Open Source Brain-Inspired Neuromorphic Software and Hardware

Jason Eshraghian

Veyepar: TalkSigns.rfxml

start: 12:57 end: 13:00 Len: 00:3:00 id: 152

Gdsfactory, an Open Source python flow for circuit design, verification and validation

Joaquin Matres

Gdsfactory, an Open Source python flow for circuit design, verification and vali

Joaquin Matres

Veyepar: TalkSigns.rfxml

start: 13:00 end: 13:03 Len: 00:3:00 id: 152

RISu064 - An in-order non-blocking dual-issue RISC-V 64 processor

Wenting Zhang

RISu064 - An in-order non-blocking dual-issue RISC-V 64 processor

Wenting Zhang

Veyepar: TalkSigns.rfxml

start: 13:03 end: 13:06 Len: 00:3:00 id: 152

SimCommand: A High-Performance RTL Testbench API with Fork/Join Support

Vighnesh Iyer

SimCommand: A High-Performance RTL Testbench API with Fork/Join Suppo

Vighnesh Iyer

Veyepar: TalkSigns.rfxml

start: 13:06 end: 13:09 Len: 00:3:00 id: 152

A radically simple 1-bit single-die "supercomputer"

James Bowman

A radically simple 1-bit single-die "supercomputer"

James Bowmar

Veyepar: TalkSigns.rfxml

start: 13:09 end: 13:12 Len: 00:3:00 id: 152

All Your OSS Codebase Are Belong To Us

Oron Port

All Your OSS Codebase Are Belong To Us

Oron Port

Veyepar: TalkSigns.rfxml

start: 13:12 end: 13:15 Len: 00:3:00 id: 152

A Modular Approach to Variable Pipeline Depth Designs

Peter Herrmann

A Modular Approach to Variable Pipeline Depth Designs

Peter Herrmann

Veyepar: TalkSigns.rfxml

start: 13:15 end: 13:18 Len: 00:3:00 id: 152

Open-source Hardware for Real-Time Applications

Francisco Wilken

Open-source Hardware for Real-Time Applications

Francisco Wilken

Veyepar: TalkSigns.rfxml

start: 13:18 end: 13:21 Len: 00:3:00 id: 152

An open-source robotics applications interface

Nikita Klimov

An open-source robotics applications interface

Nikita Klimov

Veyepar: TalkSigns.rfxml

start: 13:21 end: 13:24 Len: 00:3:00 id: 152

DSAGEN: Democratizing Domain-Specific Accelerator Generation for FPGA Overlays

Dylan Kupsh

DSAGEN: Democratizing Domain-Specific Accelerator Generation for FPGA O

Dylan Kupsh

Veyepar: TalkSigns.rfxml

start: 13:24 end: 13:27 Len: 00:3:00 id: 152

Educational Framework for Functional Verification

Matthew Michilot

Educational Framework for Functional Verification

Matthew Michilot

Veyepar: TalkSigns.rfxml

start: 13:27 end: 13:30 Len: 00:3:00 id: 152

Using CVA6 in Architecture Education

Ethan Sifferman

Using CVA6 in Architecture Education

Ethan Sifferman

Veyepar: TalkSigns.rfxml

start: 13:30 end: 13:50 Len: 00:20:00 id: 152

Open tools for an open standard: Control/status register automation using SystemRDL

Alex Mykyta

Open tools for an open standard: Control/status register automation using Syst

Alex Mykyta

Veyepar: TalkSigns.rfxml

start: 14:00 end: 14:20 Len: 00:20:00 id: 152.

Goodbye Make, Hello SiliconCompiler!

Andreas Olofsson

Goodbye Make, Hello SiliconCompiler!

Andreas Olofsson

Veyepar: TalkSigns.rfxml

start: 15:00 end: 15:20 Len: 00:20:00 id: 152

Chipyard: An Open-Source RISC-V SoC Design Framework

Abraham Gonzalez

Chipyard: An Open-Source RISC-V SoC Design Framework

Abraham Gonzale

Veyepar: TalkSigns.rfxml

start: 15:30 end: 15:50 Len: 00:20:00 id: 152

SVA based Checker IP in Verilator

Balram, Srinivasan Venkataramanan

SVA based Checker IP in Verilator

Balram, Srinivasan Venkataramanan

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:20 Len: 00:20:00 id: 152

Quality of Life with Virtual Prototypes - Open Source Tools in the Ecosystem of the RISC-V VP

Pascal Pieper

Quality of Life with Virtual Prototypes - Open Source Tools in the Ecosystem o

Pascal Pieper

Veyepar: TalkSigns.rfxml

start:09:00 end:09:20 Len: 00:20:00 id: 152

Constellation: A Open-Source Chisel Generator for Network-on-Chip Interconnects

Jerry Zhao

Constellation: A Open-Source Chisel Generator for Network-on-Chip Interconn

Jerry Zhao

Veyepar: TalkSigns.rfxml

start:09:30 end:09:50 Len: 00:20:00 id: 152

SystemVerilog-Style Constraints and Functional Coverage in Python

Matthew Ballance

SystemVerilog-Style Constraints and Functional Coverage in Python

Matthew Ballance

Veyepar: TalkSigns.rfxml

start: 10:00 end: 10:20 Len: 00:20:00 id: 152

OpenROAD - Turning Designs into Optimized Silicon

Matt Liberty

OpenROAD - Turning Designs into Optimized Silicon

Matt Liberty

Veyepar: TalkSigns.rfxml

start: 11:00 end: 11:20 Len: 00:20:00 id: 152

Space - Opportunities, Challenges for Open Source Community

CHINH LE

Space - Opportunities, Challenges for Open Source Community

CHINH LE

Veyepar: TalkSigns.rfxml

start: 11:00 end: 11:20 Len: 00:20:00 id: 152

Online Waveform viewer. Why do we need one?

Aliaksei Chapyzhenka

Online Waveform viewer. Why do we need one?

Aliaksei Chapyzhenka

Veyepar: TalkSigns.rfxml