

start: **18:00** end: **18:03** Len: 00:3:00 id: 153

set page 1 of 45

CitizenSilicon: towards an open-source Czochralski furnace for Si growth

Max Aalto

CitizenSilicon: towards an open-source Czochralski furnace for Si growth

Max Aalto

start: **18:00**

end: **18:03**

Len: 00:3:00

id: 153

set page 2 of 45

Building an Ecosystem for Hardware Generators

Rachit Nigam

Building an Ecosystem for Hardware Generators

Rachit Nigam

start: **18:00** end: **18:03**

Len: 00:3:00

id: 153

set page 3 of 45

Application of AI-computer vision based software

Max Faramarzi

Application of AI-computer vision based software

Max Faramarzi

start: **18:14** end: **18:17**

Len: 00:3:00

id: 153

set page 4 of 45

Tim's Silicon Presentations

Tim Ansell

Tim's Silicon Presentations

Tim Ansell

start: **18:18** end: **18:21**

Len: 00:3:00

id: 153

set page 5 of 45

Surfer - An Extensible and Snappy Waveform Viewer

Frans Skarman

Surfer - An Extensible and Snappy Waveform Viewer

Frans Skarman

start: **18:21**

end: **18:24**

Len: 00:3:00

id: 153

set page 6 of 45

Clean up your EDA flows with tclint

Noah Moroze

Clean up your EDA flows with tclint

Noah Moroze

start: **18:24** end: **18:27**

Len: 00:3:00

id: 153

set page 7 of 45

Attempts to design hardware using dafny

Ben Reynwar

Attempts to design hardware using dafny

Ben Reynwar

start: **18:27**

end: **18:30**

Len: 00:3:00

id: 153

set page 8 of 45

Zeno: An Open-Source Scalable Capability-Based Secure Architecture

Alan Ehret

Zeno: An Open-Source Scalable Capability-Based Secure Architecture

Alan Ehret

start: **18:29** end: **18:32**

Len: 00:3:00

id: 153

set page 9 of 45

Accelerating Hardware Design with Custom GPTs

Prakash Shvetank

Accelerating Hardware Design with Custom GPTs

Prakash Shvetank

start: **18:32**

end: **18:35**

Len: 00:3:00

id: 153

set page 10 of 45

OSHHISS Open Source for Hybrid Hetrogenous Integrated Semiconductor Systems

John Goodenough

OSHHISS Open Source for Hybrid Hetrogenous Integrated Semiconductor Sys

John Goodenoug

start: **18:35** end: **18:38**

Len: 00:3:00

id: 153

set page 11 of 45

Where Community Powers Innovation

Mohamed Kassem

Where Community Powers Innovation

Mohamed Kassem

start: 18:40

end: 18:43

Len: 00:3:00

id: 153

set page 12 of 45

CoreScore like never before

Olof Kindgren

CoreScore like never before

Olof Kindgren

start: **18:43**

end: **18:46**

Len: 00:3:00

id: 153

set page 13 of 45

ChipWhisperer: Past & Future of a FPGA-based Research Tool

Jean-Pierre Thibault

ChipWhisperer: Past & Future of a FPGA-based Research Tool

Jean-Pierre Thibault

start: 19:07

end: 19:08

Len: 00:00:20

id: 154

set page 14 of 45

clock

ck

clock

ck

start: **09:20** end: **09:40**

Len: 00:20:00 id: 153

set page 15 of 45

Caster: An Open-source E-Ink Controller

Wenting Zhang

Caster: An Open-source E-Ink Controller

Wenting Zhang

start: **09:40** end: **10:00**

Len: 00:20:00 id: 153

set page 16 of 45

Teaching Modern EDA using a Tapeout-Centric University Course

Anish Singhani

Teaching Modern EDA using a Tapeout-Centric University Course

Anish Singhani

start: **10:20** end: **10:40**

Len: 00:20:00 id: 153

set page 17 of 45

CedarEDA for open source silicon

Keno Fischer

CedarEDA for open source silicon

Keno Fischer

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end: 11:00

Len: 00:20:00

id: 153

set page 18 of 45

Cohort: Software-Oriented Acceleration for You, Me, and Our Heterogeneous SoCs

Nazerke Turtayeva

Cohort: Software-Oriented Acceleration for You, Me, and Our Heterogeneous S

Nazerke Turtayeva

start: **10:53** end: **11:13**

Len: 00:20:00 id: 153

set page 19 of 45

Towards Cycle-accurate Simulation of xBGAS

Jie Li

Towards Cycle-accurate Simulation of xBGAS

Jie Li

start: **11:00**

end: **11:20**

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set page 20 of 45

Towards xBGAS on CHERI: Examining the Benefits of a Secure Distributed Architecture

Mert Side

Towards xBGAS on CHERI: Examining the Benefits of a Secure Distributed Ar

Mert Side

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set page 21 of 45

Artifact Evaluation for the Field Programmable Gate Array Community

Miriam Leeser

Artifact Evaluation for the Field Programmable Gate Array Community

Miriam Leeser

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Len: 00:20:00

id: 153

set page 22 of 45

Chisel 6 and beyond

Jack Koenig

Chisel 6 and beyond

Jack Koenig

start: **13:20** end: **13:40** Len: 00:20:00 id: 153

set page 23 of 45

MRPHS: Enabling Transaction-level Deductive Formal Verification Through PDVL

Tobias Strauch

MRPHS: Enabling Transaction-level Deductive Formal Verification Through PC

Tobias Strauch

Veyepar: TalkSigns.rfxml

start: **14:20**

end: **14:40**

Len: 00:20:00

id: 153

set page 24 of 45

Architecture 2.0: Toward Open Source Foundation Models and Datasets for Hardware Design

Vijay Janapa Reddi, Shvetank Prakash

Architecture 2.0: Toward Open Source Foundation Models and Datasets for Hardware Design

Vijay Janapa Reddi, Shvetank Prakash

start: **14:40** end: **15:00**

Len: 00:20:00 id: 153

set page 25 of 45

Riding The Wave: Building Wave Pipelines in FPGAs

Rice Shelley

Riding The Wave: Building Wave Pipelines in FPGAs

Rice Shelley

start: **15:00** end: **15:20**

Len: 00:20:00 id: 153

set page 26 of 45

Giving Students A Byte of Open-Source: Advancing Hardware Education

Ethan Sifferman

Giving Students A Byte of Open-Source: Advancing Hardware Education

Ethan Sifferman

start: **15:40** end: **16:00**

Len: 00:20:00 id: 153

set page 27 of 45

Open-source resources for learning the Bluespec HL-HDLs

Rishiyur Nikhil

Open-source resources for learning the Bluespec HL-HDLs

Rishiyur Nikhil

start: **16:00** end: **16:20**

Len: 00:20:00 id: 153

set page 28 of 45

PyHDL-IF: An Easy-to-Use Python/HDL Cross-Calling Interface

Matt Ballance

PyHDL-IF: An Easy-to-Use Python/HDL Cross-Calling Interface

Matt Ballance

start: **09:00** end: **09:20**

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set page 29 of 45

Open source RTL verification with Verilator

Karol Gugala

Open source RTL verification with Verilator

Karol Gugala

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set page 30 of 45

Sonata: A development platform to enable exploring the use of CHERI for embedded applications

Hugo McNally

Sonata: A development platform to enable exploring the use of CHERI for emb

Hugo McNally

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set page 31 of 45

Transparent Checkpointing for Fault Tolerance in RISC-V

Aayushi Gautam

Transparent Checkpointing for Fault Tolerance in RISC-V

Aayushi Gautam

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id: 153

set page 32 of 45

HDLAgent, Enhancing Hardware Language in the age of LLMs

Jose Renau

HDLAgent, Enhancing Hardware Language in the age of LLMs

Jose Renau

start: **10:40** end: **11:00**

Len: 00:20:00 id: 153

set page 33 of 45

Spade: An HDL Inspired By Modern Software Languages

Frans Skarman

Spade: An HDL Inspired By Modern Software Languages

Frans Skarman

start: **11:00** end: **11:20**

Len: 00:20:00 id: 153

set page 34 of 45

Switchboard: Calling All Hardware Models

Steven Herbst

Switchboard: Calling All Hardware Models

Steven Herbst

start: **12:20**

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id: 153

set page 35 of 45

From an Open-Source ISA to Open-Source HW to Open-Source Silicon

Luca Bertaccini

From an Open-Source ISA to Open-Source HW to Open-Source Silicon

Luca Bertaccini

start: **12:40** end: **13:00**

Len: 00:20:00 id: 153

set page 36 of 45

Open Source Hardware: Hacking Silicon for Fun (instead of profit)

Troy Benjegerdes

Open Source Hardware: Hacking Silicon for Fun (instead of profit)

Troy Benjegerdes

start: **13:00**

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set page 37 of 45

A History of TL-Verilog Google Summer of Code Projects under FOSSi Foundation

Steve Hoover

A History of TL-Verilog Google Summer of Code Projects under FOSSi Founda

Steve Hoover

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set page 38 of 45

UMI: Universal Memory Interface

Andreas Olofsson

UMI: Universal Memory Interface

Andreas Olofsson

start: **14:20** end: **14:40**

Len: 00:20:00 id: 153

set page 39 of 45

ABC: The Way It Should Have Been Designed

Alan Mishchenko

ABC: The Way It Should Have Been Designed

Alan Mishchenko

start: **14:40** end: **15:00**

Len: 00:20:00 id: 153

set page 40 of 45

BYOL (Build Your Own Linter) – UVMLint for IEEE-UVM core code development

Ajeetha Kumari Venkatesan

BYOL (Build Your Own Linter) – UVMLint for IEEE-UVM core code developme

Ajeetha Kumari Venkatesan

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set page 41 of 45

Beyond EDA lies Edalize

Olof Kindgren

Beyond EDA lies Edalize

Olof Kindgren

start: **15:40** end: **16:00**

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set page 42 of 45

RF Front-end receiver design for 2.4GH/5GHz WiFi application

Jabeom Koo

RF Front-end receiver design for 2.4GH/5GHz WiFi application

Jabeom Koo

start: **16:00** end: **16:20**

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set page 43 of 45

CACE Study: Open source analog and mixed-signal design flow

Tim Edwards

CACE Study: Open source analog and mixed-signal design flow

Tim Edwards

start: **16:20** end: **16:40** Len: 00:20:00 id: 153

set page 44 of 45

IHP Open Source PDK: Announcement, Setup, Current State and Experiences, and look ahead

Frank Vater

IHP Open Source PDK: Announcement, Setup, Current State and Experiences

Frank Vater

start: **16:40** end: **17:00**

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set page 45 of 45

Tiny Tapeout: custom silicon open to all

Pat Deegan

Tiny Tapeout: custom silicon open to all

Pat Deegan