start: 18:00 end: 18:03 Len: 00:3:00 id: 153

Application of AI-computer vision based software

Max Faramarzi

Application of AI-computer vision based software

Max Faramarzi

Veyepar: TalkSigns.rfxml

start: 18:00 end: 18:03 Len: 00:3:00 id: 153

CitizenSilicon: towards an open-source Czochralski furnace for Si growth

Max Aalto

CitizenSilicon: towards an open-source Czochralski furnace for Si growth

Max Aalto

Veyepar: TalkSigns.rfxml

start: 18:00 end: 18:03 Len: 00:3:00 id: 153

Building an Ecosystem for Hardware Generators

Rachit Nigam

Building an Ecosystem for Hardware Generators

Rachit Nigam

Veyepar: TalkSigns.rfxml

start: 18:14 end: 18:17 Len: 00:3:00 id: 153

Tim's Silicon Presentations

Tim Ansell

Tim's Silicon Presentations

Tim Ansell

Veyepar: TalkSigns.rfxml

start: 18:18 end: 18:21 Len: 00:3:00 id: 153

Surfer - An Extensible and Snappy Waveform Viewer

Frans Skarman

Surfer - An Extensible and Snappy Waveform Viewer

Frans Skarman

Veyepar: TalkSigns.rfxml

start: 18:21 end: 18:24 Len: 00:3:00 id: 153

Clean up your EDA flows with tclint

Noah Moroze

Clean up your EDA flows with tclint

Noah Moroze

Veyepar: TalkSigns.rfxml

start: 18:24 end: 18:27 Len: 00:3:00 id: 153

Attempts to design hardware using dafny

Ben Reynwar

Attempts to design hardware using dafny

Ben Reynwar

Veyepar: TalkSigns.rfxml

start: 18:27 end: 18:30 Len: 00:3:00 id: 153

Zeno: An Open-Source Scalable Capability-Based Secure Architecture

Alan Ehret

Zeno: An Open-Source Scalable Capability-Based Secure Architecture

Alan Ehret

Veyepar: TalkSigns.rfxml

start: 18:29 end: 18:32 Len: 00:3:00 id: 153

Accelerating Hardware Design with Custom GPTs

Prakash Shvetank

Accelerating Hardware Design with Custom GPTs

Prakash Shvetank

Veyepar: TalkSigns.rfxml

start: 18:32 end: 18:35 Len: 00:3:00 id: 153

OSHHISS Open Source for Hybrid Hetrogenous Integrated Semiconductor Systems

John Goodenough

OSHHISS Open Source for Hybrid Hetrogenous Integrated Semiconductor Sys

John Goodenoug

Veyepar: TalkSigns.rfxml

start: 18:35 end: 18:38 Len: 00:3:00 id: 153

Where Community Powers Innovation

Mohamed Kassem

Where Community Powers Innovation

Mohamed Kasse

Veyepar: TalkSigns.rfxml

start: 18:40 end: 18:43 Len: 00:3:00 id: 153

CoreScore like never before

Olof Kindgren

CoreScore like never before

Olof Kindgren

Veyepar: TalkSigns.rfxml

start: 18:43 end: 18:46 Len: 00:3:00 id: 153

ChipWhisperer: Past & Future of a FPGA-based Research Tool

Jean-Pierre Thibault

ChipWhisperer: Past & Future of a FPGA-based Research Tool

Jean-Pierre Thibault

Veyepar: TalkSigns.rfxml

start: 19:07 end: 19:08 Len: 00:00:20 id: 154

clock

ck

clock

ck

Veyepar: TalkSigns.rfxml

start:09:20 end:09:40 Len: 00:20:00 id: 153

Caster: An Open-source E-Ink Controller

Wenting Zhang

Caster: An Open-source E-Ink Controller

Wenting Zhang

Veyepar: TalkSigns.rfxml

start:09:40 end:10:00 Len: 00:20:00 id: 153

Teaching Modern EDA using a Tapeout-Centric University Course

Anish Singhani

Teaching Modern EDA using a Tapeout-Centric University Course

Anish Singhani

Veyepar: TalkSigns.rfxml

start: 10:20 end: 10:40 Len: 00:20:00 id: 153

CedarEDA for open source silicon

Keno Fischer

CedarEDA for open source silicon

Keno Fischer

Veyepar: TalkSigns.rfxml

start: 10:40 end: 11:00 Len: 00:20:00 id: 153

Cohort: Software-Oriented Acceleration for You, Me, and Our Heterogeneous SoCs

Nazerke Turtayeva

Cohort: Software-Oriented Acceleration for You, Me, and Our Heterogeneous S

Nazerke Turtayeva

Veyepar: TalkSigns.rfxml

start: 10:53 end: 11:13 Len: 00:20:00 id: 153

Towards Cycle-accurate Simulation of xBGAS

Jie Li

Towards Cycle-accurate Simulation of xBGAS

Jie Li

Veyepar: TalkSigns.rfxml

start: 11:00 end: 11:20 Len: 00:20:00 id: 153

Towards xBGAS on CHERI: Examining the Benefits of a Secure Distributed Architecture

Mert Side

Towards xBGAS on CHERI: Examining the Benefits of a Secure Distributed Ar

Mert Side

Veyepar: TalkSigns.rfxml

start: 12:40 end: 13:00 Len: 00:20:00 id: 153

Artifact Evaluation for the Field Programmable Gate Array Community

Miriam Leeser

Artifact Evaluation for the Field Programmable Gate Array Community

Miriam Leeser

Veyepar: TalkSigns.rfxml

start: 13:00 end: 13:20 Len: 00:20:00 id: 153

Chisel 6 and beyond

Jack Koenig

Chisel 6 and beyond

Jack Koenig

Veyepar: TalkSigns.rfxml

start: 13:20 end: 13:40 Len: 00:20:00 id: 153

MRPHS: Enabling Transaction-level Deductive Formal Verification Through PDVL

Tobias Strauch

MRPHS: Enabling Transaction-level Deductive Formal Verification Through PD

Tobias Strauch

Veyepar: TalkSigns.rfxml

start: 14:20 end: 14:40 Len: 00:20:00 id: 153

Architecture 2.0: Toward Open Source Foundation Models and Datasets for Hardware Design

Vijay Janapa Reddi, Shvetank Prakash

Architecture 2.0: Toward Open Source Foundation Models and Datasets for Ha

Vijay Janapa Reddi, Shvetank Prakash

Veyepar: TalkSigns.rfxml

start: 14:40 end: 15:00 Len: 00:20:00 id: 153

Riding The Wave: Building Wave Pipelines in FPGAs

Rice Shelley

Riding The Wave: Building Wave Pipelines in FPGAs

Rice Shelley

Veyepar: TalkSigns.rfxml

start: 15:00 end: 15:20 Len: 00:20:00 id: 153

Giving Students A Byte of Open-Source: Advancing Hardware Education

Ethan Sifferman

Giving Students A Byte of Open-Source: Advancing Hardware Education

Ethan Sifferman

Veyepar: TalkSigns.rfxml

start: 15:40 end: 16:00 Len: 00:20:00 id: 153

Open-source resources for learning the Bluespec HL-HDLs

Rishiyur Nikhil

Open-source resources for learning the Bluespec HL-HDLs

Rishiyur Nikhil

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:20 Len: 00:20:00 id: 153

PyHDL-IF: An Easy-to-Use Python/HDL Cross-Calling Interface

Matt Ballance

PyHDL-IF: An Easy-to-Use Python/HDL Cross-Calling Interface

Matt Ballance

Veyepar: TalkSigns.rfxml

start:09:00 end:09:20 Len: 00:20:00 id: 153

Open source RTL verification with Verilator

Karol Gugala

Open source RTL verification with Verilator

Karol Gugala

Veyepar: TalkSigns.rfxml

start:09:20 end:09:40 Len: 00:20:00 id: 153

Sonata: A development platform to enable exploring the use of CHERI for embedded applications

Hugo McNally

Sonata: A development platform to enable exploring the use of CHERI for emb

Hugo McNally

Veyepar: TalkSigns.rfxml

start:09:40 end:10:00 Len: 00:20:00 id: 153

Transparent Checkpointing for Fault Tolerance in RISC-V

Aayushi Gautam

Transparent Checkpointing for Fault Tolerance in RISC-V

Aayushi Gautam

Veyepar: TalkSigns.rfxml

start: 10:20 end: 10:40 Len: 00:20:00 id: 153

HDLAgent, Enhancing Hardware Language in the age of LLMs

Jose Renau

HDLAgent, Enhancing Hardware Language in the age of LLMs

Jose Renau

Veyepar: TalkSigns.rfxml

start: 10:40 end: 11:00 Len: 00:20:00 id: 153

Spade: An HDL Inspired By Modern Software Languages

Frans Skarman

Spade: An HDL Inspired By Modern Software Languages

Frans Skarman

Veyepar: TalkSigns.rfxml

start: 11:00 end: 11:20 Len: 00:20:00 id: 153

Switchboard: Calling All Hardware Models

Steven Herbst

Switchboard: Calling All Hardware Models

Steven Herbst

Veyepar: TalkSigns.rfxml

start: 12:20 end: 12:40 Len: 00:20:00 id: 153

From an Open-Source ISA to Open-Source HW to Open-Source Silicon

Luca Bertaccini

From an Open-Source ISA to Open-Source HW to Open-Source Silicon

Luca Bertaccini

Veyepar: TalkSigns.rfxml

start: 12:40 end: 13:00 Len: 00:20:00 id: 153

Open Source Hardware: Hacking Silicon for Fun (instead of profit)

Troy Benjegerdes

Open Source Hardware: Hacking Silicon for Fun (instead of profit)

Troy Benjegerdes

Veyepar: TalkSigns.rfxml

start: 13:00 end: 13:20 Len: 00:20:00 id: 153

A History of TL-Verilog Google Summer of Code Projects under FOSSi Foundation

Steve Hoover

A History of TL-Verilog Google Summer of Code Projects under FOSSi Founda

Steve Hoover

Veyepar: TalkSigns.rfxml

start: 13:20 end: 13:40 Len: 00:20:00 id: 153

UMI: Universal Memory Interface

Andreas Olofsson

UMI: Universal Memory Interface

Andreas Olofsson

Veyepar: TalkSigns.rfxml

start: 14:20 end: 14:40 Len: 00:20:00 id: 153

ABC: The Way It Should Have Been Designed

Alan Mishchenko

ABC: The Way It Should Have Been Designed

Alan Mishchenko

Veyepar: TalkSigns.rfxml

start: 14:40 end: 15:00 Len: 00:20:00 id: 153

BYOL (Build Your Own Linter) – UVMLint for IEEE-UVM core code development

Ajeetha Kumari Venkatesan

BYOL (Build Your Own Linter) – UVMLint for IEEE-UVM core code developme

Ajeetha Kumari Venkatesan

Veyepar: TalkSigns.rfxml

start: 15:00 end: 15:20 Len: 00:20:00 id: 153

Beyond EDA lies Edalize

Olof Kindgren

Beyond EDA lies Edalize

Olof Kindgren

Veyepar: TalkSigns.rfxml

start: 15:40 end: 16:00 Len: 00:20:00 id: 153

RF Front-end receiver design for 2.4GH/5GHz WiFi application

Jabeom Koo

RF Front-end receiver design for 2.4GH/5GHz WiFi application

Jabeom Koo

Veyepar: TalkSigns.rfxml

start: 16:00 end: 16:20 Len: 00:20:00 id: 153

CACE Study: Open source analog and mixed-signal design flow

Tim Edwards

CACE Study: Open source analog and mixed-signal design flow

Tim Edwards

Veyepar: TalkSigns.rfxml

start: 16:20 end: 16:40 Len: 00:20:00 id: 153

IHP Open Source PDK: Announcement, Setup, Current State and Experiences, and look ahead

Frank Vater

IHP Open Source PDK: Announcement, Setup, Current State and Experiences

Frank Vater

Veyepar: TalkSigns.rfxml

start: 16:40 end: 17:00 Len: 00:20:00 id: 153

Tiny Tapeout: custom silicon open to all

Pat Deegan

Tiny Tapeout: custom silicon open to all

Pat Deegan

Veyepar: TalkSigns.rfxml